AMENDMENT TO THE CLAIMS

1. (Currently amended) A semiconductor apparatus comprising:

a plurality of nodes;

a plurality of [[serially-connected]] bodies are connected in series and ~~comprised of a switch element and a resistance element~~ respectively interposed between the [[a]] plurality of nodes [[terminals adjacent to one another]], each body having a switch element and a resistance element which are connected in series;

a plurality of test terminals for a conduction test respectively connected to one and another ends of the [[a]] plurality [[series]] of [[the serially-connected]] bodies; and

a switch control terminal for a collective control connected to ~~collectively controlling~~ all the ~~plural~~ plurality of switch elements.

2. (Currently amended) A semiconductor apparatus as claimed in Claim 1, wherein each resistance value of the plurality of [[plural]] resistance elements in the plurality ~~a series~~ of ~~the plural serially-connected~~ bodies is weighted.

3-14. (Canceled)

15. (Currently amended) A semiconductor apparatus as claimed in Claim 1 ~~any of claims 1, 3, 4, 7, 8, 11, 12, 13 and 14~~ wherein

the switch elements are formed from N-type or P-type MOS transistors, or N-type and P-type MOS transistors.

16. (Currently amended) A semiconductor apparatus as claimed in Claim 1 ~~any of claims 1, 3, 5, 7, 11, 12, 13 and 14~~ wherein

the resistance elements are formed from N-type or P-type transistors, or N-type and P-type MOS transistors.